



Designing with Multi-Gigabit Serial I/O

RIO22000-10-ILT (v1.0)

Course Specification

Course Description

Learn how to employ RocketIO™ GTP and GTX serial transceivers in your Virtex®-5 LXT, SXT, FXT, or TXT FPGA design. Understand and utilize the features of the RocketIO transceiver blocks, such as CRC, 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection. Additional topics include use of the Architecture Wizard, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

Level – Intermediate

Course Duration – 3 days

Price –

Course Part Number – RIO22000-10-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog or VHDL experience (or the *Introduction to Verilog* or the *Introduction to VHDL* course)
- Familiarity with logic design (state machines and synchronous design)
- Basic knowledge of Virtex-5 FPGA architecture and Xilinx implementation tools is helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Xilinx ISE® Foundation™ software 10.1
- ChipScope™ Pro software 10.1
- Mentor Graphics ModelSim simulator

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the ports and attributes of the RocketIO multi-gigabit transceiver in the Virtex-5 FPGA
- Effectively utilize the following features of the GTP/GTX:
 - 8B/10B and other encoding/decoding, comma detection, CRC, clock correction, and channel bonding
 - Pre-emphasis and linear equalization
- Use the GTP/GTX Transceiver Wizard to instantiate GTP and GTX primitives in a design
- Access appropriate reference material for board design issues involving the power supply, oscillators, and trace design

Course Outline

Day 1

- Virtex-5 Family Overview
- GTP Overview
- GTP Clocking and Resets
- 8B/10B Encoder and Decoder
- **Lab 1:** 8B/10B Disparity and Bypass
- Commas and Deserializer Alignment
- **Lab 2:** Commas and Data Alignment
- RX Elastic Buffer and Clock Correction

Day 2

- **Lab 3:** Clock Correction
- Channel Bonding
- **Lab 4:** Channel Bonding
- Cyclical Redundancy Check
- **Lab 5:** Cyclical Redundancy Check

- GTP Wizard Overview
- Implementing and Simulating a RocketIO Transceiver Design
- **Lab 6:** Synthesis and Implementation
- Physical Media Attachments

Day 3

- GTP Board Design
- Differences Between the GTX and GTP Transceivers
- 64B/66B Encoding and the Gearbox
- **Lab 7:** 64B/66B GTX Transceiver
- RocketIO Transceiver Test and Debugging
- **Lab 8:** ChipScope Pro Serial I/O Toolkit and IBERT
- RocketIO Transceiver Application Examples

Lab Descriptions

- **Lab 1:** 8B/10B Disparity and Bypass – Utilize the 8B/10B encoder and decoder and observe running disparity. Learn how to bypass the 8B/10B encoder and decoder.
- **Lab 2:** Commas and Data Alignment – Use programmable comma detection to align a serial data stream.
- **Lab 3:** Clock Correction – Utilize the attributes and ports associated with clock correction to compensate for frequency differences in the TX and RX clocks.
- **Lab 4:** Channel Bonding – Modify a design to use two transceivers bonded together to form one virtual channel.
- **Lab 5:** Cyclical Redundancy Check – Create design modules that include the dedicated CRC blocks in the Virtex-5 FPGA.
- **Lab 6:** Synthesis and Implementation – Use the GTP Wizard to configure RocketIO transceiver primitives. Instantiate the resulting component in a design, synthesize the design, and implement the design.
- **Lab 7:** 64B/66B GTX Transceiver – Generate a 64B/66B GTX core by using the CORE Generator™ tool, simulate the design, and analyze the results.
- **Lab 8:** ChipScope Pro Serial I/O Toolkit and IBERT – Use the ChipScope Pro Serial I/O Toolkit to verify a GTP link.

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