



Designing a LogiCORE PCI Express System

PCIE28000-92-ILT (v1.0)

Course Specification

Course Description

Attending the *Designing a LogiCORE PCI Express System* will provide you a working knowledge of how to implement a Xilinx PCI Express® core in your applications. This course focuses on the implementation of a Xilinx PCI Express system with supporting logic and example designs. With this experience, you can improve your time to market with your PCIe core design. Various Xilinx PCI Express core products will be enumerated to aid you in selecting the proper solution. This course focuses on the Virtex™-5 FPGA PCIe Endpoint Block Plus and the Spartan™-3 PCIe integrated Endpoint PIPE block.

Level – Intermediate

Course Duration – 2 days

Price –

Course Part Number – PCIE28000-92-ILT

Who Should Attend?

- Hardware designers who want to create applications using Xilinx IP cores for PCI Express
- Software engineers who want to understand the deeper workings of the Xilinx LogiCORE PCI Express solution
- System architects who want to leverage key Xilinx advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites

- Comprehensive understanding of the PCIe protocol (2 hour review included)
- Solid knowledge of Verilog or VHDL
- Solid experience with commonly used simulation tools such as Mentor Graphics ModelSim or ISIM
- Basic knowledge of Xilinx ISE™ software
- *Designing for Performance and Designing with Multi-Gigabit Serial I/O* are recommended

Software Tools

- Xilinx ISE 9.2i
- ISIM 9.2i
- ChipScope Pro 9.2i

After completing this comprehensive training, you will have the necessary skills to:

- Construct a basic PCIe system:
 - Select the appropriate core for your application
 - Specify and design an example endpoint application
 - Connect the PCIe core with the user endpoint functionality
 - Utilize FPGA resources to support the core
 - Simulate the design
 - Develop a software application to drive an endpoint
- Identify the advanced capabilities of the PCIe specification protocol and feature set

Course Outline

Day 1

- Course Introduction
- Review of the PCIe System Architecture and Protocol
- PCIe and CORE Generator
- **Lab 1:** Constructing the PCIe Core
- Simulating a PCIe Design
- Connecting Logic to the Core – Local Link
- **Lab 2a:** Downstream Port Model Simulation

- Designing the Endpoint Application
- **Lab 2b:** Pseudo-Transactional Modeling

Day 2

- **Lab 3:** Implementing the Design
- Compliance and Debugging
- **Lab 4:** Debugging the PCIe Core with the ChipScope Pro Tools
- Errors and Interrupts
- Host Side –Applications and Drivers
- **Lab 5:** Running the System
- Mechanicals, Hot Plug, and Power
- Course Summary

Lab Descriptions

- **Lab 1: Constructing the PCIe Core:** Familiarizes you with all the necessary flow of the Xilinx CORE Generator™ software for generating a Xilinx LogiCORE™ Endpoint Block Plus IP. You will select appropriate parameters for the CORE Generator tool and create the PCIe core used throughout the labs
- **Labs 2 a and b - Simulating the PCIe Core:** Provides an overview of simulating the core using the ISIM tool. You will observe and capture the effects of link training and write packets to the endpoint application during the Downstream Port Model simulation. This data will be played back during a transactional module simulation lab.
- **Lab 3: Implementing the Design:** Familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream.
- **Lab 4: Debugging Strategies:** Using a traffic simulator, you will use the ChipScope™ Pro tools to monitor the behavior of the core and the endpoint application for proper operation.
- **Lab 5: Running the Application:** You will modify C code to target the Configuration Space of the design that was implemented in the previous lab and execute an example program to exercise the endpoint.

Register Today

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