

## Course Description

This course demonstrates how to use the ISE®, PlanAhead™, and Embedded Development Kit (EDK) software tools to construct, implement, and download a Partially Reconfigurable (PR) FPGA design. You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow.

This course covers both the tool flow and mechanics of successfully creating a PR design. It also describes several techniques focusing on appropriate coding styles for a PR system as well as system-level design considerations and practical applications.

**Level** – FPGA 4

**Course Duration** – 2 days

**Course Part Number** – FPGA31000-12-ILT

**Who Should Attend?** – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and the Xilinx design methodology and who have need of partial reconfiguration techniques

### Prerequisites

- *Essentials of FPGA Design* course
- *Designing for Performance* course
- *Advanced FPGA Implementation* course
- Working HDL knowledge (VHDL or Verilog)

### Recommended

- *Embedded Systems Development* course
- *Designing with the PlanAhead Analysis and Design Tool* course

### Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 12.1 with PR license

After completing this comprehensive training, you will have the necessary skills to:

- Build and assemble a Partially Reconfigurable system
- Define PR regions and reconfigurable modules with the PlanAhead software
- Generate the appropriate bitstreams targeting Platform Flash and System ACE™ interface tool files to support on-board partial bitstream storage
- Identify how Partial Reconfiguration affects various silicon resources, including block RAM, IOBs, fabric, and MGTs
- Implement a PR system using the following techniques:
  - Direct JTAG connection
  - HDL state machines
  - Timing constraints and analysis
  - Microprocessor-based designs

## Course Outline

### Day 1

- Course Introduction
- Partial Reconfiguration Methodology
- **Lab 1:** Partial Reconfiguration Flow
- Partial Reconfiguration Design Recommendations
- Partial Reconfiguration Tool Flow
- Optional: FPGA Configuration Overview
- Partial Reconfiguration Bitstreams
- **Lab 2:** Building an HDL ICAP Controller

### Day 2

- Managing Clock Resources
- Managing Timing
- **Lab 3:** Partial Reconfiguration Timing Analysis and Constraints
- Embedded Environment (EDK)
- **Lab 4:** EDK Partial Reconfiguration
- Partial Reconfiguration Debugging
- PCIe Core and Partial Reconfiguration
- Course Summary

## Lab Descriptions

- **Lab 1:** Partial Reconfiguration Flow – Illustrates the basic PlanAhead tool Partial Reconfiguration flow. At the completion of this lab, you will download partial bitstream to the ML605 board via the JTAG connection.
- **Lab 2:** Building an HDL ICAP State Machine – Illustrates how Platform Flash can be used to store both the initial full bitstream as well as a number of partial bitstreams and how a simple HDL state machine can load the partial bitstreams on command.
- **Lab 3:** Partial Reconfiguration Timing Analysis and Constraints – Shows how area groups and reconfigurable partitions affect design performance. TPSYNC is used to reduce the impact of partitioning on timing.
- **Lab 4:** EDK Partial Reconfiguration – Demonstrates low-latency techniques via an embedded MicroBlaze™ processor and a custom ICAP loader. All aspects of completing a full embedded PR design are covered, including the embedded hardware design, software development, and implementing reconfigurable partitions. This design leverages the System ACE interface to store partial bitstreams.

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