

Course Description

Interested in learning how to effectively utilize Virtex®-5 FPGA architectural resources? Targeted towards experienced Xilinx users who have already completed *Essentials of FPGA Design* and *Designing for Performance*, this course focuses on understanding as well as designing into several of the resources found in this popular device.

Topics covered include a Virtex-5 FPGA overview, the CLB, DCM and PLL, global and regional clocking techniques, memory, DSP and arithmetic logic, and source-synchronous resources. The resources available in the LXT and SXT platforms (EMAC, the PCI Express® architecture, and GTP transceivers) are also discussed. In addition, you will learn about the resources included in the TXT and FXT platforms (GTX transceivers and the PowerPC® processor). A combination of modules and labs allow for practical hands-on application of the principles taught.

Level – FPGA 3

Course Duration – 1 day

Price –

Course Part Number – V5-21000-11-ILT

Who Should Attend? – For those who have taken the *Essentials of FPGA Design* and *Designing for Performance* courses.

Prerequisites

- *Essentials of FPGA Design* course
- *Designing for Performance* course

Software Tool

- Xilinx ISE® Design Suite: System Edition 11.1

After completing this comprehensive training, you will have the necessary skills to:

- Describe the 6-input LUT of the Virtex-5 FPGA
- Specify the CLB arrangement in the Virtex-5 FPGA
- Define the block RAM resources of the Virtex-5 FPGA
- Differentiate the arithmetic logic resources of the DSP48E slice in the Virtex-5 FPGA
- Identify the clocking resources of the Virtex-5 FPGA
- Describe the additional features of the Virtex-5 LXT, SXT, FXT, and TXT FPGA platforms

Course Outline

- Introduction
- Virtex-5 FPGA Overview
- CLB Resources
- Clocking Resources
- **Lab 1:** Clocking Resources
- I/O Resources
- Memory Resources
- XtremeDSP Solution Resources
- **Lab 2:** DSP48E Resources
- Virtex-5 LXT, SXT, FXT, and TXT FPGA Overview
- **Lab 3:** (Optional) DSP48E Resources

Lab Descriptions

The labs will provide practical hands-on application of the principles taught throughout the course.

Lab 1: Clocking Resources – In this lab, you will use the Architecture Wizard to create a PLL core for instantiation in your design. You will then simulate and verify the PLL core.

Lab 2: DSP48E Resources – In this lab, you will create a MACC and a loadable MACC by using the XtremeDSP™ solution (DSP48E) resource through the CORE Generator™ software. You will then compare the OPMODEs chosen by the CORE Generator software with the expected values.

Lab 3: DSP48E Resources – The DSP48E resource in the Virtex-5 FPGA can also be utilized to create non-DSP functions in order to save slice resources. In this optional lab, you will create a multiplexer by using the XtremeDSP solution (DSP48E) resource through primitive instantiation. You will then simulate the resources to verify functionality.

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